**AMENDMENTS TO THE SPECIFICATION**:

Please replace paragraph [0014] with the following:

[0014] The output from the RF stage is down converted using a free running local oscillator. The receiver local oscillator is free running and therefore there is usually an offset frequency from that of the transmitter local oscillator. Here is where a timing estimation and correction is done. The output from the down converter is sampled and converted to digital at an analog to digital ~~concerted~~convertor (A/D) 29 passes to a Fast Fourier Transform module (FFT) 31 through time domain processing 30. The output from the FFT 31 is applied to the frequency domain processing 33. The output from the FFT is processed for channel compensation due to wireless channel fading, timing errors and frequency offset. The output samples from the FFT 31 are applied to a single clock enabled module 35 enabled for channel estimation and pilot processing. The output from the channel estimation and pilot processing module 35 is applied to time domain processing 30 and frequency domain processing 33. The output from the frequency domain processing 33 is demodulated through demodulation stage 37 and then is decoded at decoder 39, descrambled at descrambler 41 and applied to the MAC interface to the user.

Please replace paragraph [0039] with the following:

[0039] In accordance with the present invention as illustrated in FIG. 3 there is provided the receiver 51 with a separate channel estimator 35a and separate pilot processing 35b and a control logic decode state machine 55 that is response to a new packet to turn on the channel estimator 35a for channel estimation time period only in the preamble and the channel estimation channel estimation module value is stored in a register and used until the start of a new packet with a preamble. FIG. 3 uses the same callouts for the same elements in FIG. 1. The elements in FIG. 3 that are now controlled are modified to be controllable. The channel estimator 35a receives the data signal sent over the channel and compares this with the known data signals stored in the receiver and determines the channel distortion. The inverse of this channel distortion is then

calculated and stored at the output register 36 of the channel estimator 35a to be used to equalize the received signal from the channel. The pilot processing 35b is used throughout the whole data portion after the preamble until the presence of a new packet. The pilot signals are at a set of four frequency bands in the received data signals.